IN THE SPECIFICATION

The paragraph beginning at page 12, line 8 is amended as follows:

Figure 3 illustrates another embodiment of a floating gate transistor, or non-volatile memory cell 300, according to the teachings of the present invention. As shown in the embodiment of Figure 3, the non-volatile memory cell 300 includes a vertical non volatile memory cell 300. In this embodiment, the non-volatile memory cell 300 has a first source/drain region 301 formed on a substrate 306. A body region 307 including a channel region 305 is formed on the first source/drain region 301. A second source/drain region 303 is formed on the body region 307. Methods for forming such a vertical transistor structure are disclosed in US Patent no. 6,135,175, entitled "Memory Address Decode Array with vertical transistors, which is incorporated herein by reference. A floating gate 309 opposes the channel region 305 and is separated therefrom by a gate oxide 311. A control gate 313 opposes the floating gate 309. According to the teachings of the present invention, the control gate 313 is separated from the floating gate 309 by a low tunnel barrier intergate insulator 315.

The paragraph beginning at page 13, line 14 is amended as follows:

Figure 4 is a perspective view illustrating an array of silicon pillars 400-1, 400-2, 400-3, . . . , 400-N, formed on a substrate 406 as used in one embodiment according to the teachings of the present invention. As will be understood by one of ordinary skill in the art upon reading this disclosure, the substrates can be (i) conventional p-type bulk silicon or p-type epitaxial layers on p+ wafers, (ii) silicon on insulator formed by conventional SIMOX, wafer bonding and etch back or silicon on sapphire, or (iii) small islands of silicon on insulator utilizing techniques, such as

SUPPLEMENTAL AMENDMENT Serial Number: 09/945512

Filing Date: August 30, 2001

Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

described in more detail in U.S. patent no. 5,691,230, by Leonard Forbes, entitled "Technique for

Producing Small Islands of Silicon on Insulator," issued 11/25/1997, which is incorporated herein by reference.

The paragraph beginning at page 16, line 13 is amended as follows:

As shown in the embodiment of Figure 5E, a single floating gate 509 is formed in each trench 530 between adjacent pillars which form memory cells 500-1 and 500-2. According to the teachings of the present invention, the single floating gate 509 can be either a vertically oriented floating gate 509 or a horizontally oriented floating gate 509 formed by conventional processing techniques, or can be a horizontally oriented floating gate 509 formed by a replacement gate technique such as described in a copending application, entitled "Flash Memory with Ultrathin Vertical Body Transistors," by Leonard Forbes and Kie Y. Ahn, application serial no. 09/780,169. In one embodiment of the present invention, the floating gate 509 has a vertical length facing the body region 505 of less than 100 nm. In another embodiment, the floating gate 509 has a vertical length facing the body region 505 of less than 50 nm. In one embodiment, as shown in Figure 5E, the floating gate 509 is shared, respectively, with the body regions 507-1 and 507-2, including channel regions 505-1 and 505-2, in adjacent pillars 500-1 and 500-2 located on opposing sides of the trench 530. And, as shown in Figure 5E, the control gate includes a single horizontally oriented control gate line, or control gate 513 formed above the horizontally oriented floating gate 509.

Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

The paragraph beginning at page 20, line 13 is amended as follows:

The tunneling current in erasing charge from the floating gate 705 by tunneling to the control gate 713 will then be as shown in Figure 7B given by an equation of the form:

$$J = B \exp(-Eo/E)$$

$$J = \frac{q^2 E^2}{4\pi h \Phi} e^{-E_0/E} \quad E_0 = \frac{8\pi}{3} \frac{\sqrt{2m q \Phi^{3/2}}}{h}$$

where E is the electric field across the interpoly dielectric insulator 707 and Eo depends on the barrier height. Practical values of current densities for a Aluminum oxide which has a current density of 1 A/cm² at a field of about $E = 1V/20A = 5x10^{+6} \text{ V/cm}_2$ -are evidenced in a description by Pollack. (See generally, S. R. Pollack and C. E. Morris, "Tunneling through gaseous oxidized films of Al₂O₃," Trans. AIME, Vol. 233, p. 497, 1965). Practical current densities for sSilicon oxide transistor gate insulators which has have a current density of 1 A/cm² at a field of about E = 2.3V/23A = 1x10⁺⁷ V/cm₋-are evidenced in a description by T.P. Ma et al.. (See generally, T. P. Ma et al., "Tunneling leakage current in ultrathin (<a4 nm) nitride/oxide stack dielectries," IEEE Electron Device Letters, vol. 19, no. 10, pp. 388-390, 1998).

The paragraph beginning at page 22, line 4 is amended as follows:

The oxide growth rate and limiting thickness will increase with oxidation (iii) temperature and oxygen pressure. The oxidation kinetics of a metal may, in some cases, depend on the crystallographic orientations of the very small grains of metal which comprise the metal film (see generally, O, Kubaschewski and B. E. Hopkins, "Oxidation of Metals and Alloys", Butterworth, London, pp. 53-64, 1962). If such effects are significant, the metal deposition process can be modified in order to increase its preferred orientation and subsequent oxide

SUPPLEMENTAL AMENDMENT Serial Number: 09/945512 Filing Date: August 30, 2001

Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

thickness and tunneling uniformity. To this end, use can be made of the fact that metal films strongly prefer to grow during their depositions having their lowest free energy planes parallel to the film surface. This preference varies with the crystal structure of the metal. For example, fcc metals prefer to form {111} surface plans. Metal orientation effects, if present, would be larger when only a limited fraction of the metal will be oxidized and unimportant when all or most of the metal is oxidized.

The paragraph beginning at page 22, line 24 is amended as follows:

This oxide barrier has been studied in detail using Pb/PbO/Pb structures. The oxide itself can be grown very controllably on deposited lead films using either thermal oxidation (see generally, J. M. Eldridge and J. Matisco, "Measurement of tunnel current density in a Meal-Oxide Metal system as a function of oxide thickness," Proc. 12th Intern. Conf. on Low

Temperature Physics, pp. 427-428, 1971; J. M. Eldridge and D. W. Dong, "Growth of thin PbO layers on lead films. I. Experiment," Surface Science, Vol. 40, pp. 512-530, 1973) or rf sputter etching in an oxygen plasma (see generally, J. H. Greiner, "Oxidation of lead films by rf sputter etching in an oxygen plasma", J. Appl. Phys., Vol. 45, No. 1, pp. 32-37, 1974). It will be seen that there are a number of possible variations on this structure. Starting with a clean poly-Si substrate, one processing sequence using thermal oxidation involves:

The paragraph beginning at page 23, line 16 is amended as follows:

(iii) Using a "low temperature oxidation process" to grow an oxide film of self-limited thickness. In this case, oxygen gas is introduced at the desired pressure in order to oxidize the lead in situ without an intervening exposure to ambient air. For a fixed oxygen pressure and

Serial Number: 09/945512

Filing Date: August 30, 2001

Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

temperature, the PbO thickness increases with log(time). Its thickness can be controlled via time or other parameters to within 0.10 A, as determined via in situ ellipsometric or ex situ measurements of Josephson tunneling currents. This control is demonstrated by the very limited statistical scatter of the current PbO thickness data shown in the insert of Fig. 3-in an article by J. M. Eldridge and J. Matisoo, entitled "Measurement of tunnel current density in a Meal-Oxide-Metal system as a function of oxide thickness," Proc. 12th Intern. Conf. on Low Temperature Physics, pp. 427-428, 1971. This remarkable degree of control over tunnel current is due to the excellent control over PbO thickness that can be achieved by "low temperature oxidation." For example, increasing the oxidation time from 100 to 1,000 minutes at an oxygen pressure of 750 Torr at 25C only raises the PbO thickness by 3 A (e.g., from ~21 to 24 A, see Fig. 1 in J. M. Eldridge and J. Matisoo, "Measurement of tunnel current density in a Meal-Oxide Metal system as a function of oxide thickness," Proc. 12th Intern. Conf. on Low Temperature Physics, pp. 427-428, 1971). Accordingly, controlling the oxidation time to within 1 out of a nominal 100 minute total oxidation time provides a thickness that is within 0.1 A of 21A. The PbO has a highly stoichiometric composition throughout its thickness, as evidenced from ellipsometry-(e.g., see Fig. 6 in J. M. Eldridge and D. W. Dong, "Growth of thin PbO layers on lead films. I. Experiment," Surface Science, Vol. 40, pp. 512-530, 1973) and the fact that the tunnel barrier heights are identical for Pb/PbO/Pb structures.

The paragraph beginning at page 25, line 1 is amended as follows:

A number of studies have dealt with electron tunneling in Al/Al₂O₃/Al structures where the oxide was grown by "low temperature oxidation" in either molecular or plasma oxygen-(see generally, S. M. Sze, Physics of Semiconductor Devices, Wiley, NY, pp. 553-556, 1981; G.

Serial Number: 09/945512

Filing Date: August 30, 2001

Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

Simmons and A. El Badry, "Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film," J. Appl. Phys., Vol. 34, p. 1793, 1963; S. R. Pollack and C. E. Morris, "Tunneling through gaseous exidized films of Al₂O₃," Trans. AIME, Vol. 233, p. 497, 1965; Z. Hurych, "Influence of nonuniform thickness of dielectric layers on capacitance and tunnel currents," Solid State Electronics, Vol. 9, p. 967, 1966; S. P. S. Arya and H. P. Singh, "Conduction properties of thin Al2O3 films," Thin Solid Films, Vol. 91, No. 4, pp. 363-374, May 1982; K.-H. Gundlach and J. Holzl, "Logarithmic conductivity of Al Al₂O₃-Al tunneling junctions produced by plasma and by thermal oxidation", surface Science, Vol. 27, pp. 125-141, 1971). Before sketching out a processing sequence for these tunnel barriers, note:

The paragraph beginning at page 25, line 19 is amended as follows:

Tunnel currents are asymmetrical in this system with somewhat larger currents (ii) flowing when electrons are injected from Al/Al₂O₃ interface developed during oxide growth. This asymmetry is due to a minor change in composition of the growing oxide: there is a small concentration of excess metal in the Al₂O₃, the concentration of which diminishes as the oxide is grown thicker. The excess Al+3 ions produce a space charge that lowers the tunnel barrier at the inner interface. The oxide composition at the outer Al₂O₃/Al contact is much more stoichiometric and thus has a higher tunnel barrier. In situ ellipsometer measurements on the thermal oxidation of A1 films deposited and oxidized in situ support this model-(see generally, J. Grimblot and J. M. Eldridge, "I. Interaction of Al films with O2 at low pressures", J. Electro. Chem. Soc., Vol. 129, No. 10, pp. 2366-2368, 1982. J. Grimblot and J. M. Eldridge, "II. Oxidation of Al films", ibid, 2369-2372, 1982). In spite of this minor complication, Al/Al₂O₃/Al tunnel barriers can be formed that will produce predictable and highly controllable tunnel

SUPPLEMENTAL AMENDMENT Serial Number: 09/945512 Filing Date: August 30, 2001

Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

currents that can be ejected from either electrode. The magnitude of the currents are still primarily dominated by Al₂O₃ thickness which can be controlled via the oxidation parametrics.

The paragraph beginning at page 26, line 8 is amended as follows:

With this background, we can proceed to outline one process path out of several that can be used to form Al₂O₃ tunnel barriers. Here the aluminum is thermally oxidized although one could use other techniques such as plasma oxidation (see generally, S. R. Pollack and C. E. Morris, "Tunneling through gaseous oxidized films of Al₂O₃," Trans. AIME, Vol. 233, p. 497, 1965; K. H. Gundlach and J. Holzl, "Logarithmic conductivity of Al Al₂O₃ Al tunneling junctions produced by plasma and by thermal oxidation", Surface Science, Vol. 27, pp. 125-141, 1971) or rf sputtering in an oxygen plasma (see generally, J. H. Greiner, "Oxidation of lead films by rf sputter etching in an oxygen plasma", J. Appl. Phys., Vol. 45, No. 1, pp. 32-37, 1974). For the sake of brevity, some details noted above will not be repeated. The formation of the Al/Al₂O₃/Al structures will be seen to be simpler than that described for the Pb/PbO/Pb junctions owing to the much higher melting point of aluminum, relative to lead.

The paragraph beginning at page 26, line 24 is amended as follows:

(ii) Oxidize the aluminum in situ in molecular oxygen using temperatures, pressure and time to obtain the desired Al₂O₃ thickness. As with PbO, the thickness increases with log (time) and can be controlled via time at a fixed oxygen pressure and temperature to within 0.10 Angstroms, when averaged over a large number of aluminum grains that are present under the counter-electrode. One can readily change the Al₂O₃ thickness from ~15 to 35A by using appropriate oxidation parametrics (e.g., see Figure 2 in J. Grimblot and J. M. Eldridge, "II.

SUPPLEMENTAL AMENDMENT Serial Number: 09/945512

Filing Date: August 30, 2001

Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

Oxidation of Al films", J. Electro. Chem. Soc., Vol. 129, No. 10, pp. 2369-2372, 1982). The oxide will be amorphous and remain so until temperatures in excess of 400C are reached. The initiation of recrystallization and grain growth can be suppressed, if desired, via the addition of small amounts of glass forming elements (e.g., Si) without altering the growth kinetics or barrier heights significantly.

The paragraph beginning at page 27, line 13 is amended as follows:

Single layers of Ta₂O₅, TiO₂, ZrO₂, Nb₂O₅ and similar transition metal oxides can be formed by "low temperature oxidation" of numerous Transition Metal (e.g., TM oxides) films in molecular and plasma oxygen and also by rf sputtering in an oxygen plasma. The thermal oxidation kinetics of these metals have been studied for decades-with numerous descriptions and references to be found in the book by Kubaschewski and Hopkins (O. Kubaschewski and B. E. Hopkins, "Oxidation of Metals and Alloys", Butterworth, London, pp. 53-64, 1962). In essence, such metals oxidize via logarithmic kinetics to reach thicknesses of a few to several tens of angstroms in the range of 100 to 300C. Excellent oxide barriers for Josephson tunnel devices can be formed by rf sputter etching these metals in an oxygen plasma (see generally, J. M. Greiner, "Josephson tunneling barriers by rf sputter etching in an oxygen plasma," J. Appl. Phys., Vol. 42, No. 12, pp. 5151-5155, 1971; O. Michikami et al., "Method of fabrication of Josephson tunnel junctions," U.S. Pat. 4,412,902, Nov. 1, 1983). Such "low temperature oxidation" approaches differ considerably from MOCVD processes used to produce these TM oxides. MOCVD films require high temperature oxidation treatments to remove carbon impurities, improve oxide stoichiometry and produce recrystallization. Such high temperature treatments also cause unwanted interactions between the oxide and the underlying silicon and thus have

SUPPLEMENTAL AMENDMENT
Serial Number: 09/945512
Filing Date: August 30, 2001
Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

necessitated the introduction of interfacial barrier layers.—See, for example, H. F. Luan et al.,

"High quality Ta₂O₃-gate dielectries with T_{ex,eq} <10 angstroms," IEDM Tech. Digest, pp. 141-

The paragraph beginning at page 28, line 6 is amended as follows:

144, 1999.

An approach was developed utilizing "low temperature oxidation" to form duplex layers of TM oxides. A new approach was described in a copending application by J. M. Eldridge, entitled "Thin Dielectric Films for DRAM Storage Capacitors," patent application Serial No. 09/651,380 filed Aug. 29, 2000 that utilizes "low temperature oxidation" to form duplex layers of TM oxides. Unlike MOCVD films, the oxides are very pure and stoichiometric as formed. They do require at least a brief high temperature (est. 700 to 800C but may be lower) treatment to transform their microstructures from amorphous to crystalline and thus increase their dielectric constants to the desired values (> 20 or so). Unlike MOCVD oxides, this treatment can be carried out in an inert gas atmosphere, thus lessening the possibility of inadvertently oxidizing the poly-Si floating gate. While this earlier disclosure was directed at developing methods and procedures for producing high dielectric constant films for storage cells for DRAMs, the same teachings can be applied to producing thinner metal oxide tunnel films for the flash memory devices described in this disclosure. The dielectric constants of these TM oxides are substantially greater (>25 to 30 or more) than those of PbO and Al₂O₃. Duplex layers of these high dielectric constant oxide films are easily fabricated with simple tools and also provide improvement in device yields and reliability. Each oxide layer will contain some level of defects but the probability that such defects will overlap is exceedingly small. Effects of such duplex layers were first reported by one J. M. Eldridge of the present authors and are well known to

Serial Number: 09/945512

Filing Date: August 30, 2001

Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS practitioners of the art. It is worth mentioning that highly reproducible TM oxide tunnel barriers can be grown by rf sputtering in an oxygen ambient, as referenced above (see generally, J. M. Greiner, "Josephson tunneling barriers by rf sputter etching in an oxygen plasma," J. Appl. Phys., Vol. 42, No. 12, pp. 5151-5155, 1971; O. Michikami et al., "Method of fabrication of Josephson tunnel junctions," U.S. Pat. 4,412,902, Nov. 1, 1983). Control over oxide thickness and other properties in these studies were all the more remarkable in view of the fact that the oxides were typically grown on thick (e.g., 5,000 A) metals such as Nb and Ta. In such metal-oxide systems, a range of layers and suboxides can also form, each having their own properties. In the present disclosure, control over the properties of the various TM oxides will be even better since we employ very limited (perhaps 10 to 100 A or so) thicknesses of metal and thereby preclude the formation of significant quantities of unwanted, less controllable sub-oxide films. Thermodynamic forces will drive the oxide compositions to their most stable, fully oxidized state, e.g., Nb₂O₅, Ta₂O₅, etc. As noted above, it will still be necessary to crystallize these duplex oxide layers. Such treatments can be done by RTP and will be shorter than those used on MOCVD and sputter-deposited oxides since the stoichiometry and purity of the "low temperature oxides" need not be adjusted at high temperature.

The paragraph beginning at page 30, line 22 is amended as follows:

Some results have been obtained which demonstrate that at least a limited range of high temperature, super-conducting oxide films can be made by thermally oxidizing Y-Ba-Cu alloy films (see generally, Hase et al., "Method of manufacturing an exide superconducting film," U.S. Pat. 5,350,738, Sept. 27, 1994). The present inventors have also disclosed how to employ "low temperature oxidation" and short thermal treatments in an inert ambient at 700C in order to form

SUPPLEMENTAL AMENDMENT Serial Number: 09/945512

Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

a range of perovskite oxide films from parent alloy films (see generally, J. M. Eldridge, "Low

Cost Processes for Producing High Quality Perovskite Dielectric Films," application Serial No.

). The dielectric constants of crystallized, perovskite oxides can be very large, with values in the 100 to 1000 or more range. The basic process is more complicated than that needed to oxidize layered films of transition metals. (See Example III.) The TM layers would typically be pure metals although they could be alloyed. The TMs are similar metallurgically as are their oxides. In contrast, the parent alloy films that can be converted to a perovskite oxide are typically comprised of metals having widely different chemical reactivities with oxygen and other common gasses. In the Y-Ba-Cu system referenced above, Y and Ba are among the most reactive of metals while the reactivity of Cu approaches (albeit distantly) those of other noble metals. If the alloy is to be completely oxidized, then thin film barriers such as Pd, Pt, etc. or their conductive oxides must be added between the Si and the parent metal film to serve as: electrical contact layers; diffusion barriers; and, oxidation stops. In such a case, the Schottky barrier heights of various TM oxides and perovskite oxides in contact with various metals will help in the design of the tunnel device. In the more likely event that the perovskite parent alloy film will be only partially converted to oxide and then covered with a second layer of the parent alloy (recall the structure of Figure 2), then the barrier heights will represent that developed during oxide growth at the parent perovskite alloy/perovskite oxide interface. Obviously, such barrier heights cannot be predicted ab initio for such a wide class of materials but will have to be developed as the need arises. This information will have to be developed on a system-by-system basis.

Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

At page 42, line 11 please add the following:

DOCUMENTS

- US Pat. 6,498,065, "Memory Address Decode Array with vertical transistors;"
- US Pat. 5,691,230, "Technique for Producing Small Islands of Silicon on Insulator;"
- US Pat. 6,424,001, "Flash Memory with Ultrathin Vertical Body Transistors;"
- S.R. Pollack and C.E. Morris, "Tunneling through gaseous oxidized films of Al₂O₃," Trans. AIME, Vol. 233, p. 497, 1965;
- O. Kubaschewski and B.E. Hopkins, "Oxidation of Metals and Alloys," Butterworth, London, pp. 53-64, 1962;
- J.M. Eldridge and J. Matisoo, "Measurement of tunnel current density in a Meal-Oxide-Metal system as a function of oxide thickness," Proc. 12th Intern. Conf. On Low Temperature Physics, pp. 427-428, 1971;
- J.M. Eldridge and D.W. Wong, "Growth of thin PbO layers on lead films. I. Experiment," Surface Science, Vol. 40, pp. 512-530, 1973;
- J.H. Greiner, "Oxidation of lead films by rf sputter etching in an oxygen plasma," J. Appl. Phys., Vol. 45, No. 1, pp. 32-37, 1974;
- S.M. Sze, Physics of Semiconductor Devices, Wiley, NY, pp. 553-556, 1981;
- G. Simmons and A. El-Badry, "Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film," J. Appl. Phys., Vol. 34, p. 1793, 1963;
- Z. Hurych, "Influence of nonuniform thickness of dielectric layers on capacitance and tunnel circuits," Solid-State Electronics, Vol. 9, p. 967, 1966;
- S.P.S. Arya and H.P. Singh, "Conduction properties of Al₂O₃ films," Thin solid Films, vol. 91, No. 4, pp. 363-374, May, 1982;

Serial Number: 09/945512

Filing Date: August 30, 2001
Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

- K.-H. Gundlach and J. Holzl, "Logarithmic conductivity of Al-Al₂O₃-AL tunneling junctions produced by plasma- and by thermal-oxidation," Surface Science, Vol. 27, pp. 125-141, 1971;
- J. Grimblot and J.M. Eldridge, "I. Interaction of Al films with O₂ at low pressures," J. Electro.

 Chem. Soc., Vol. 129, No. 10, pp. 2366-2368, 1982;
- J. Grimblot and J.M. Eldridge, "II. Oxidation of Al films," J. Electro. Chem. Soc., Vol. 129, No. 10, pp. 2369-2372, 1982;
- J.M. Greiner, "Josephson tunneling barriers by rf sputter etching in an oxygen plasma," J. Appl.

 Phys., Vol. 42, No. 12, pp. 5151-5155, 1971;
- US Patent 4,412,902, "Method of fabrication of Josephson tunnel junction;"
- H.F. Luan et al., "High quality Ta₂O₅ gate dielectrics with T_{ox,eq}<10 angstroms," IEDM Tech Digest, pp. 141-144, 1999;
- US Patent 6,461,931, "Thin dielectric films for DRAM storage capacitors;"
- US Patent 5,350,738, "Method of manufacturing an oxide superconducting film;"
- T.P. Ma et al., "Tunneling leakage current in ultrathin (<a4 nm) nitride/oxide stack dielectrics,"

 IEEE Electron Device Letters, vol. 19, no. 10, pp/ 388-390, 1998;

Scrial Number: 09/945512 Filing Date: August 30, 2001

Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

Respectfully Submitted,

LEONARD FORBES

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 349-9587

Date 24 500 3

Timothy B. Chse

Reg. No. 40,957

CERTIFICATE UNDER 37 CFR § 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelop addressed to: Commissioner for Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 24th day of September 2003.

Name Amy Moriarty

Signature